

MAURICIO KUGLER

Contact Information

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Personal Information

Date of Birth: April 9th, 1978

Place of Birth: Curitiba, Paraná, Brazil

Parents: Walter Kugler and Gisela Kugler

Citizenship: Brazilian

Educational Record

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| 2003 - 2007 | Ph.D. in Pattern Recognition, Department of Computer Science & Engineering, Nagoya Institute of Technology, Nagoya, Japan. |
| 2001 - 2003 | M.Sc. in Biomedical Engineering, Graduate School in Electrical Engineering and Industrial Computer Science, Federal Technological University of Paraná, Curitiba, Brazil. |
| 1996 - 2000 | B.E. in Electrical Engineering - emphasis in Electronics & Telecommunication, Department of Electronics, Federal Technological University of Paraná, Curitiba, Brazil. |
| 1993 - 1996 | High School, Technician in Electronics, Department of Electronics, Federal Technological University of Paraná, Curitiba, Brazil. |

Academic Experience

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| 2007 - | Assistant Professor, Department of Computer Science and Engineering, Nagoya Institute of Technology (NITech), Nagoya, Japan. |
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- 2011 - Invited Lecturer, Biomedical Signal Processing (30 hours), Biomedical Engineering Program, École Supérieure d'Ingénieurs en Génie Électrique (ESIGELEC), Rouen, France.
- 2011 - Invited Lecturer, Digital Signal Processors (20 hours), Embedded Systems Program, École Supérieure d'Ingénieurs en Génie Électrique (ESIGELEC), Rouen, France.

Professional Experience

- 2007 - Assistant Professor, Department of Computer Science & Engineering Nagoya Institute of Technology, Nagoya, Japan.
- 2001 - 2003 Internship, LIT - Laboratory of Innovation and Technology in Embedded Systems Federal Technological University of Paraná, Curitiba, Brazil.
- 1999 Internship, Siemens Telecommunications, Curitiba, Brazil.
- 1998 - 1999 Internship, NuPES - Concurrent Engineering R&D Laboratory, Federal Technological University of Paraná, Curitiba, Brazil.
- 1997 Internship - MMA2 Project, SIEMENS & CEFET-PR partnership, Federal Technological University of Paraná, Curitiba, Brazil.

Grants And Scholarships

- 2013 - 2014 Research Grant from the Japan Society for the Promotion of Science, TANAKA, S. and KUGLER, M., *Development of a wearable brain stimulation device for gait rehabilitation.*
- 2013 - 2014 Research Grant from the Japan Society for the Promotion of Science, MASATOKI, S. and KUGLER, M. *Sound visualization system based on a head mount display.*
- 2005 Research grant from The Hori Information Science Promotion Foundation.
- 2003 - 2007 Monbukagakusho Scholarship from the Ministry of

Education, Science, Sports and Culture of Japan.

Honors And Awards

- 2008 Best Paper Award in the 15th International Conference on Neural Information Processing.
- 2000 First Place among graduating students in Electrical Engineering, Federal Technological University of Paraná, Curitiba, Brazil.

Events Participation

- 2010 Paper Presentation in the 20th International Conference on Artificial Neural Networks, Thessaloniki.
- 2008 Session Chair & Paper Presentation in the 15th International Conference on Neural Information Processing, Auckland.
- 2007 Session Co-Chair & Paper Presentation in the 14th International Conference on Neural Information Processing, Kitakyushu.
- 2006 Poster presentation in the 14th European Symposium on Artificial Neural Networks, Bruges, Belgium.
- 2004 Poster presentation in the 8th Pacific Rim International Conference on Artificial Intelligence, Auckland, New Zealand.
- 2002 Paper presentation in the 18th Brazilian Congress of Biomedical Engineering, São José dos Campos, Brazil.
- 2001 Assistant National Leader of the Brazilian Delegation, The 14th Ship for World Youth Program, sponsored by Cabinet Office, Government of Japan, Tokyo, Japan.

Important Publications[†]

Thesis

- [1] M. Kugler. *Large-Scale Divide-and-Conquer Support Vector Classification*. PhD thesis, Graduate School of Engineering, Department

[†]For the complete list of publications, please access:
<http://www.mauriciokugler.com/publications.html>

of Computer Science and Engineering, Nagoya Institute of Technology, Nagoya, February 2007. 135 pages.

- [2] M. Kugler. *Contribution to the development of brain-computer interfaces using visually evoked potentials* Master's thesis, Graduate School in Electrical Engineering and Industrial Computer Science, Federal Technological University of Parana, Curitiba, February 2003. 170 pages.

Journals and Conferences

- [3] M. Kugler, T. Tossavainen, M. Nakatsu, S. Kuroyanagi, and A. Iwata. Real-time Hardware Implementation of a Sound Recognition System With In-Field Learning. *IEICE Transactions on Information & Systems*, E99-D(7):1885–1894, July 2016.
- [4] H. Tsuzuki, M. Kugler, S. Kuroyanagi, and A. Iwata. An Approach for Sound Source Localization by Complex-Valued Neural Network. *IEICE Transactions on Information & Systems*, E96-D(10):2257–2265, October 2013.
- [5] M. Kugler, T. Hishida, S. Kuroyanagi, and A. Iwata. A Novel Approach for Hardware Based Sound Localization. *Proceedings of the 20th International Conference on Artificial Neural Networks*, pages 490–499, Thessaloniki, Springer Verlag, 2010, Part II, LNCS 6352.
- [6] M. Kugler, V. Benso, S. Kuroyanagi, and A. Iwata. Novel Approach for Hardware Based Sound Classification. *Proceedings of the 15th International Conference on Neural Information Processing*, pages 859–866, Auckland, Springer Verlag, 2009, Part II, LNCS 5507.
- [7] M. Kugler, S. Kuroyanagi, A. S. Nugroho, and A. Iwata. CombNET-III with nonlinear gating network and its application in large-scale classification problems. *IEICE Transactions on Information & Systems*, E91-D(2):286–295, February 2008.
- [8] M. Kugler and H. S. Lopes. A configware approach for the implementation of a LVQ neural network. *International Journal of Computational Intelligence Research*, 3(1):21–25, January 2007.
- [9] M. Kugler, S. Kuroyanagi, A. S. Nugroho, and A. Iwata. CombNET-III: a support vector machine based large scale classifier with probabilistic framework. *IEICE Transactions on Information & Systems*, E89-D(9):2533–2541, September 2006.

Patents

- [10] S. Masatoki, M. Kugler, K. Fukaya, and J. Makovníková. *A head-mounted display capable of detecting hazardous events based on sound localization and recognition*. Patent Number: 2015-12863, Applicant: Nagoya Institute of Technology, 2015, Japan.
- [11] M. Kugler and A. Iwata. *Sound source identification method and sound source identification device*. Patent Number: 2010-79188, Applicant: Nagoya Institute of Technology, 2010, Japan.

Lectures

Biomedical Signal Processing (ESIGELEC)

Digital signal processing applied to biomedical signals, signal acquisition, sampling theorem, time analysis, frequency analysis, digital filters, basic algorithms for electrocardiogram and electroencephalogram signal processing.

Digital Signal Processors (ESIGELEC)

Introduction to the usage of floating-point digital signal processors TMS320C6713 from Texas Instruments, TMS320C6713 architecture, hardware parallelism, floating point notation, basic review digital signal processing, implementation of digital filters and signal synthesis.

Introduction to Image Processing - Laboratory (NITech)

Introduction to image processing basic methods, data structures for image representation, image rotation, translation and scaling, color manipulation, circular buffer for temporal processing.

Digital Circuits - Laboratory (NITech)

Basics of digital circuits, Boolean algebra, numerical bases, digital gates, flip-flops, digital counters.

Project Development - Laboratory (NITech)

Students are divided in teams and have 6 months to develop a project that uses knowledge acquired during the course (software or hardware development). The project is required to have a minimal level of complexity and concepts of project management have to be applied along the development.

Important Projects

2014 -

Wearable Sound Localization Assistive Device for the Hearing Impaired

Development of wearable aiding systems capable of recognizing and localizing a small set of sounds. One of the designs focus on the type of sound source and it consists on an digital microphone and an RGB LED, both mounted directly in a glass-like frame. A patent application was recently submitted and the electronics for an initial proof-of-concept version is already being developed, along with initial 3D-printed mechanical parts. The second design consists in a head-mount display, which contains a pair of microphones and a camera facing backwards, which, together with battery and mass storage, are all embedded on the glasses frames. When a sound is recognized and localized to be on the back, the system alerts the user, and when the user stops walking, the image of the rear-facing camera is displayed to the user eyes. A patent of this design was submitted and approved in 2015. The last design consists of a glass frame capable of full-plane sound localization. The four microphones place on the corner of the frame combine the multiple time-delays of each pair of microphones in order to calculate, in real time, the direction of the sound source. A new mathematical model was developed to combine the extracted angles in a final direction, and a scientific paper was submitted in 2016.

2014 - 2015

Wearable Brain Stimulation Device for Gait Rehabilitation

Development of a portable device that generates a programmable constant current on the scalp of a subject. This stimulation is used on gait rehabilitation, which consists on the process of re-learning how to walk after an injury or with a disability. My participation on the project consists on the hardware and firmware development of such device. The project includes analog electronics and digital circuit design. Such design is challenging; not only it involves complex analog circuits for generating the desired stimulation, but it is also supposed to present very reduces dimensions, as it is supposed to be fixed in a cap wore by the subject. Also for the same reason, the device must be controlled wirelessly by a smartphone or tablet device.

2008 - 2013

Sound Recognition Support System for the Hearing Impaired

Portable device capable of recognizing up to nine different environmental sounds and informing the user about the occurrence of the sound event in real-time. This information is done by several interfaces, in-

cluding a Bluetooth link to Android-based smartphones. The system can also learn new sounds by itself, without the need of a host computer. The hardware is based in a Field-Programmable Gate Array (FPGA) device, instead of a conventional microcontroller. This choice is justified by the high computational complexity of the signal processing operations required to achieve a high performance in the sound recognition. The prototypes were completely developed by our team, including the schematics design, components selection, printed circuit board design, FPGA firmware development and case design.

Professional Affiliations

2005 - The Institute of Electrical & Electronics Engineers (IEEE).

Foreign Languages

Portuguese (native)
English (fluent)
Japanese (intermediate)
Spanish (intermediate)

Computer Skills

Operating System: Microsoft Windows, Linux, Android.
Programming Languages: C, C++, C#, Java, PHP, Assembler, VHDL, MATLAB.

Personal References

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Federal University of Technology - Paraná
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Extra Professional Activities

Music: Clarinet and Bass Clarinet player.